

10/517258

Rev. 1/16/01

Effective March 1998

## DECLARATION AND POWER OF ATTORNEY FOR U. S. PATENT APPLICATION

☒ Original ☐ Supplemental ☐ Substitute ☐ PCT ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, DATA STORAGE VERIFICATION DEVICE, AND DATA STORAGE VERIFICATION METHOD ✓

of which is described and claimed in:

☐ the attached specification, or

☐ the specification in the application Serial No. \_\_\_\_\_ filed \_\_\_\_\_; and with amendments through \_\_\_\_\_ (if applicable), or

☒ the specification in International Application No. PCT/JP03/07541 ✓, filed June 13, 2003, and as amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any application(s) for patent or inventor's certificate listed below and have also identified below any application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
<u>Japan</u> ✓	<u>2002-174883</u> ✓	<u>June 14, 2002</u> ✓	<u>Yes</u>


I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

10/517258

6- And I hereby appoint Michael R. Davis, Reg. No. 25,134; Matthew M. Jacob, Reg. No. 25,154; Warren M. Cheek, Jr., Reg. No. 33,367; Nils Pedersen, Reg. No. 33,145; Charles R. Watts, Reg. No. 33,142; and Michael S. Huppert, Reg. No. 40,268, who together constitute the firm of WENDEROTH, LIND & PONACK, L.L.P., as well as any other attorneys and agents associated with Customer No. 000513, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys and agents named herein to accept and follow instructions from Hayase & Co. as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

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1-00

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10/517258

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I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor Katsuhiko Nakai Date Nov. 11. 2004  
 2nd Inventor Tsuyoshi Namba Date Nov. 11. 2004  
 3rd Inventor Takehisa Hirano Date Nov. 11. 2004  
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 7th Inventor \_\_\_\_\_ Date \_\_\_\_\_

The above application may be more particularly identified as follows:

U.S. Application Serial No. \_\_\_\_\_ Filing Date \_\_\_\_\_  
 Applicant Reference Number P-30917-01 Atty Docket No. \_\_\_\_\_  
 Title of Invention SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, DATA STORAGE VERIFICATION DEVICE,  
AND DATA STORAGE VERIFICATION METHOD